ADS78/8509 EVM User's Guide

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1 Introduction

The ADS7809 and ADS8509 are complete 16-bit analog-to-digital (A/D) using state-of-the-art CMOS structures. They contain a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or can be synchronized to an external data clock. The ADS7809 and ADS8509 also provide an output synchronization pulse for ease of use with standard DSP processors.

The EVM is available with either the ADS7809 or ADS8509 installed. The EVM can also accommodate the 12-bit ADS7808 simply removing and replacing the installed device. Samples of the ADS7808 can be obtained through the sample program at Texas Instruments. See the ADS7808 Product Folder for details.

1.1 Features

- Full-Featured Evaluation Board for the ADS7808, ADS7809 or ADS8509, serial Analog to Digital Converters
- 4 V, 5 V, 10 V, ±3.3 V, ±5 V and ±10 V Analog Input Ranges
- Built in reference
- High-Speed Serial Interface
- Compatible with the 5-6K Interface Board for use with a variety of DSP Starter Kits as well as the HPA449 from SoftBaugh, Inc. (www.softbaugh.com).
- Field Programmable Gate Array (FPGA) users can evaluate the ADS78/8509 EVM by obtaining the Texas Instruments Analog Adapter Kit from Avnet Design Services (www.em.avnet.com).

2 Analog Interface

For maximum flexibility, the ADS78/8509 EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Please consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 shows the pin out of the analog input connector, J1.

Table 1. Pinout of the Analog Input Connector, J1

Pin Number	Signal	Description
J1.2 thru J1.16 (even)	Analog Input	To accommodate EVM Stacking using the TAG feature of the data converter, jumper W12 can be used in combination with J1 to choose one of eight analog input channels to the evaluation module.
J1.20	REF(+)J	External reference source input, accessible through W6.
J1.15	REFOUT	Optional connection via W6. Provides external AFE circuitry with REFOUT bias voltage.
J1.1- J1.19 (odd)	AGND	Analog ground connections. Note J1.15 is used for REFOUT connections to external AFE circuitry.

The analog front-end (AFE) circuitry found on the EVM consists of a simple RC filter. When used in combination with the 5-6K Interface Board, the circuits found on both DAP Signal Conditioning Boards (see SLAU105) provide the level shifting and amplifier configurations to realize single ended or bi-polar mode operation of the analog-to-digital converter installed on the EVM.

2.1 Analog Input Range Selection

Jumpers W1 through W5 provide a convenient way to choose the analog input range. W1 controls the input connection to pin 1 (R1IN), W2 controls the connection to pin 3 (R2IN) and W3 controls the inputs on pins 4 and 5 (R3IN and CAP). Jumpers W4 and W5 provide connections to 33.2K resistors wired to the CAP pin and TRIM adjustment pot R6 (via W5). Table 2 is representative of the input range selection.

Table 2. Input Range Selection(1)

Range	Without Trim					With Trim				
	W1	W2	W3	W4	W5	W1	W2	W3	W4	W5
0–10 V	5–6	1–2	5–6	1–2	2–3	5–6	1–2	5–6	1–2	1–2
0–5 V	5–6	5–6	1–2	1–2	2–3	5–6	5–6	1–2	1–2	1–2
0–4 V	1–2	5–6	1–2	2–3	2–3	1–2	5–6	1–2	2–3	1–2
±10 V	5–6	5–6	3–4	2–3	2–3	5–6	5–6	3–4	2–3	1–2
±5 V	1–2	1–2	3–4	1–2	2–3	1–2	1–2	3–4	1–2	1–2
±5 V	1–2	1–2	3–4	2–3	2–3	1–2	1–2	3–4	2–3	1–2

(1) For Offset Adjustment, close W6 pins 5–6 and adjust R8 before trimming.

2.2 Optional Amplifier Input

Jumper W7 provides access to an optional amplifier/buffer circuit on the front end of the data converter. Component U2 can be installed at the user's option with any standard 8 pin SOIC single amplifier component. The amplifier circuit is connected to the ±VA terminals for split supply operation. If single supply amplifiers are used, the –VA (J3 pin 2) can be tied to analog ground (J3 pin 6). The footprint for common 4mm trim pots (see component R11) is provided as an offset adjustment pot for single supply amplifiers. When used in conjunction with the 5-6K Interface Board, please be aware that the –VA supply is common to all power connectors (JP1 through JP6). Shorting the –VA supply to ground on the ADS78/8509 EVM is possible only if it is not used elsewhere on the interface board.

3 Digital Interface

The ADS78/8509 EVM is designed for easy interfacing to multiple control platforms. Jumper options are provided on the EVM to allow direct control over the serial clock source as well as the data output and TAG features.

The active low $\overline{CS0}$ pin is connected to J2 pin 1. This pin can be controlled through GPIO functions on the 5–6K Interface Board or the HPA449. For standalone operation, a shunt jumper can be placed between J2T pins 1 and 2 to tie $\overline{CS}$ to ground.

The DATA output from the EVM is applied to W9. When the supplied shunt is on pins 1-2 (default state), the DATA output is fed to J2B (bottom side) pin 11. This is required when operating in the internal data clock mode, where the ADC supplies an SPI master clock to the host processor. Data is input to the SIMO pin of the host in this case. W13 is provided as a means to return the ADC generated SPI clock to DSP host processors using the 5-6K Interface Board.

3.1 Using TAG Features via W8, W9, and W10

W8 controls the TAG function of the ADC. With the supplied shunt in position 1-2 (default state), TAG is grounded and the EVM is to be considered as either the only converter in the system, or the LAST converter in the data chain (see SBAA007 for additional details). When the shunt on W8 is moved to position 2–3, data input to the TAG pin is fed from J2T (top side) pin 13. W8 and W9 must be in position 1-2 for the last converter in the chain and position 2–3 for all other devices when using the TAG feature. The TAG feature also requires the use of an external data clock. W10 sets the EXT/INT pin high (external clock) when the pins are open (no shunt installed). The external data clock can be applied to J2 pin 3 (top or bottom side).

3.2 Additional Digital Control and Monitoring

As mentioned previously, W10 controls the selection of the internal or external data clock. When W10 is closed (default) the ADC generates a low dwelling burst mode clock that allows the user to read valid data on either the rising or falling edge. Removing the shunt from W10 requires an external data clock applied to J2 pin 3 (top or bottom side) to produce a data output stream. W11 controls the data format; when closed (default) the DATA output pin provides a Binary Twos Complement data stream. Opening W11 provides a straight binary output of the conversion results. W14 controls the device power down function. Opening W14 applies a logic high to the PWRD pin, shutting down the ADC. W14 can be wired to GPIO output J2 pin 19 for use with the HPA449 board.

Test points TP4 and TP6 provide access to the SYNC and BUSY signals respectively. These can be monitored by referencing an oscilloscope to TP5, digital ground (labeled DGND). The applied digital voltage can be monitored at TP3. Analog signals and the applied VANA voltage can be monitored at TP2 (+5V) referenced to TP1 (AGND).

4 Power Supplies

The ADS78/8509 EVM board requires +5V DC for both the analog and digital sections of the ADC. Power to the ADC is sourced from J3 pin 3 and pin 10 (+5VA and +5VD - see table below).

Note:
VDIG must be less than or equal to VANA.

The following table shows the pin out of J3:

Table 3. Pinout of J3

Signal	Pin Number		Signal
+VA	1	2	-VA

Table 3. Pinout of J3 (continued)

Signal	Pin Number		Signal
+5VA	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
Unused	9	10	+5VD

For stand alone operation, power sources can be applied via various test points located on the EVM (VANA to TP2 and VDIG to TP3). Refer to the schematic at the end of this document for details.

The option amplifier located at position U2 (user supplied) can be powered through J3 pins 1 and 2. See the earlier discussion about the power supply restrictions in section 1.2 of this manual.

Note:
While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

4.1 Reference Voltage control via W6

The ADS78/8509 is normally configured to use its internal reference. Jumper W6 provides various options to allow the EVM user to send the converter's reference voltage off board to external amplifier circuits (W6 pins 3-4, default state). An external reference sourceapplied to J1 pin 20 can be sent to the ADC by moving the shunt at W6 to pins 1-2. An on board trim pot is provided at R8, and can be used with a shunt jumper placed on W6 pins 5–6.

5 EVM Operation

The max analog input swing is +/-10Vpp. The input range can be adjusted directly on the EVM by configuring jumpers W1 through W5, with offset trim capability using W6. The EVM is set for the 0-10V input range by default with the serial data stream supplied by the internal clock. Offset trim can be accomplished on board via R8 or through an external input through J1. Single amplifier U2 in an industry standard SOIC 8 package can be installed to do on board signal conditioning if necessary. Please refer to Section 12 of Op Amps for Everyone (Doc. No. SLOD006) for information on various circuit applications.

Once power is applied to the EVM, the analog input source can be connected directly to J1 (top or bottom side) or through optional amplifier and signal conditioning modules using the 5-6K Interface Board or HPA449. Jumper W12 allows the EVM user to choose which analog signal applied to J1 is directed to the input of the ADC, providing the ability to stack up to eight ADS78/8509 EVM's using the TAG features of the device. When using the TAG feature, be sure to set the jumpers according to section 2.1 of this Users Guide.

The digital control signals can be applied directly to J2 (top or bottom side). The ADS78/8509 EVM can also be connected directly to the 5-6K Interface Board for use with a variety of C5000 and C6000 series DSP Starter Kits (DSK). The analog and digital input connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon type cables on 0.1" centers.

No specific evaluation software is provided with this EVM, however, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments Incorporated. Check the product folders or send e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are available on request.

Table 4 shows the factory default jumper locations for the ADS78/8509 EVM:

Table 4. Factory Default Jumper Locations

Jumper	Function	Default Condition
W1	Controls application of the applied analog signal to R1IN	5–6
W2	Controls application of the applied analog signal to R2IN	1–2
W3	Controls application of the applied analog signal to R3IN	5–6
W4	Controls connection of 33.2 kΩ resistors to the CAP pin and TRIM pot	1–2
W5	Controls connection of 33.2 kΩ resistors to the CAP pin and TRIM pot	2–3
W6	Controls the application of the reference voltage	3–4
W7	Controls the application of optional signal conditioning circuitry	1–2
W8	Controls the TAG feature	1–2
W9	Controls the application of the DOUT data stream	1–2
W10	Controls the EXT/INT clock pin	CLOSED
W11	Controls the SB/BTC data format pin	CLOSED
W12	Used to select an analog input channel when used with DAP Signal Conditioning Boards	1–2
W13	Controls the application of clock return for DSP receiver operations	CLOSED
W14	Controls the PWRD function	CLOSED

6 EVM Bill of Materials and Schematic

Table 5 contains a complete Bill of Materials for the ADS78/8509EVM. The schematic diagram is also provided for reference.

Table 5. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1	2.2 nF, 0805, X7R, 50V	Panasonic	ECJ-2VB1H222K
C2 C9	2.2 µF, 0805, X5R, 10V	TDK	C2012X5R1A225K/0.85
C3 C4	10 µF 0805, X5R, 10V	Murata	GRM21BR61A106KE19L
C5 C7	10 µF Tant., A case, 10V	Panasonic	ECS-T1AY106R
C6 C12	0.1µF, X7R, 25V	TDK	C2012X7R1E104K
C8 C10 C11 C13	0.01 µF, X7R, 25V	Panasonic	ECJ-2VB1H103K
J1 J2 (top side)	10 pin, dual row, SMTheader (20 pos.)	Samtec	TSM-110-01-T-DV-P
J1 J2 (bottom side)	10 pin, dual row, SMT socket (20 pos.)	Samtec	SSW-110-22-F-D-VS-K
J3 (top side)	5 pin, dual row, SMT header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
J3 (bottom side)	5 pin, dual row, SMT socket (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
L1 L2	15 µH inductor, SMT, 1608 series	Inductors, Inc.	CTDS1608C-153
R1 R4	100 Ω, 0805, 1%	Yageo America	9C08052A1000FKHFT
R2	576 kΩ, 0805, 1%	Yageo America	9C08052A5763FKHFT
R3 R5	33.2 kΩ, 0805, 1%	Yageo America	9C08052A3322FKHFT
R6 R8	50 kΩ, SMT Trim Pot, 4mm	Bourns	3214W-1-503E
R7	200 Ω, 0805, 1%	Yageo America	9C08052A1002JLHFT
R12 R13 R14	10 kΩ, 0805, 5%	Yageo America	9C08052A1002JLHFT
R15	33 Ω, 0805, 5%	Yageo America	9C08052A33R0JLHFT
R9	0 Ω, 0805, 5%	Yageo America	9C08052A0R00JLHFT
R10, R11, R16, R17	Not Installed		

Table 5. Bill of Materials (continued)

Designators	Description	Manufacturer	Mfg. Part Number
TP2 TP3	Red test point loop	Keystone	5000
TP1 TP5 TP4 TP6	Black test point loop	Keystone	5001
U1	ADS7809 or ADS8509	TI	ADS7809U or ADS8509U
U2	Not Installed	TI	Single Op Amp - SOIC
W1 W2 W3 W6	3 pin, dual row, TH header (6 pos.)	Samtec	TSW-103-07-L-D
W4 W5 W7 W8 W9	3 pin , 0.1" header	Samtec	TSW-103-07-L-S
W10 W11 W13 W14	2 pin , 0.1" header	Samtec	TSW-102-07-L-S
W12	8 pin , dual row, 2mm header (16 pos)	Samtec	TMM-108-02-L-D

7 Related Documentation from Texas Instruments

Table 6. EVM Compatible Device Data Sheets, Users Guides and Additional Resources

Data Sheet	Literature Number
ADS7808	SBAS018
ADS7809	SBAS017
ADS8509	SLAS324
Users Guides	**Literatuare Number**
5-6K Interface Board	SLAU104
DAP Signal Conditioning Boards	SLAU105
Additional Resources	**Literature Number**
Op Amps for Everyone	SLOD006
ADS7809 TAG Features	SBAA007

RANGE	W/O TRIM					W/TRIM				
	W1	W2	W3	W4	W5	W1	W2	W3	W4	W5
0-10V	5-6	1-2	5-6	1-2	2-3	5-6	1-2	5-6	1-2	1-2
0-5V	5-6	5-6	1-2	1-2	2-3	5-6	5-6	1-2	1-2	1-2
0-4V	1-2	5-6	1-2	2-3	2-3	1-2	5-6	1-2	2-3	1-2
+/-10V	1-2	5-6	3-4	2-3	2-3	1-2	5-6	3-4	2-3	1-2
+/-5V	5-6	1-2	3-4	1-2	2-3	5-6	1-2	3-4	1-2	1-2
+/-3V	1-2	1-2	3-4	2-3	2-3	1-2	1-2	3-4	2-3	1-2

FOR OFFSET ADJUST, MOVE W6 to position 5-6

Revision History		
REV	ECN Number	Approved
1	Prototype	TH
A	Initial Release	TH

Operating Modes:
Internal Clock (SPI Master) - W10 Closed, W8 1-2, W9 1-2
External Clock (No TAG) - W10 Open, W8 1-2, W9 2-3
External Clock (W/ TAG) - W10 Open, W8 2-3 (1-2 Last Board), W9 2-3

J1 EVM_IN_0 EVM_IN_1 EVM_IN_2 EVM_IN_3 EVM_IN_4 EVM_IN_5 EVM_IN_6 EVM_IN_7

W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14

R1 100 ohm
R2 576K
R3 33.2K
R4 100 ohm
R5 33.2K
R6 50K
R7 200 ohm
R8 50K
R9 0 Ohm
R10
R11
R12 10K
R13 10K
R14 10K
R15 33
R16
R17

C1 2.2nF
C2 2.2uF
C3 10uF
C4 10uF
C5
C6 0.1uF
C7
C8 0.01uF
C9 2.2uF
C10 10nF
C11 10nF
C12 0.1uF
C13 0.01uF

L1 15uH
L2 15uF

U1
R1IN R2IN R3IN CAP REF Vana AGND1 AGND2 /CS DATACLK R/C SYNC DATA TAG /BUSY EXT/INT SB/BTC PWRD VDIG DGND

U2

J2B /CS SCLK CLKR FSX FSR SIMO DR /INT TOUT GPIO

J2T /CS SCLK FSX TAG TOUT GPIO

J3 DGND AGND

TP1 TP2 TP3 TP4 TP5 TP6

EXT_REFIN REFOUT ADJ_REFIN ADC_ANALOG_IN

+VA -VA 5Va 5Vd +5VA +5VD

Drawn By:	Tom Hendrick
Engineer:	Tom Hendrick
FILE:	EDGE #6465121

TEXAS INSTRUMENTS
12500 TI Blvd. Dallas, Texas 75243

Title: ADS7809/8509 Evaluation Module Schematic

SIZE: B | DATE: 30-Oct-2004 | REV: A | SHEET: 1 OF: 1

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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It is important to operate this EVM within the input voltage range of 0 V to 15 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30 C. The EVM is designed to operate properly with certain components above 60 C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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